I claim:

1. A method for determining a pattern of output bits from an integrated circuit comprising:

obtaining a sequence of logic transitions that are a function of one or more bits from the integrated circuit;

determining a transition time of each logic transition in the sequence of logic transitions; and

deriving the pattern of output bits from the integrated circuit as a function of the transition time of each logic transition in the sequence of logic transitions.

2. The method of claim 1 further comprising the operation of:

comparing the pattern of output bits from the integrated circuit with an expected pattern of output bits.

3. The method of claim 1 wherein the operation of determining a transition time of each logic transition further comprises:

generating a plurality of transition time windows, each transition time window comprising a range of time when a logic transition of a bit of the pattern of output bits is expected; and

assigning each logic transition of the sequence of logic transitions to one of the plurality of transition time windows.

4. The method of claim 3 wherein the range of time for each transition window comprises:

a minimum time when the logic transition of a bit may be assigned to the transition window;

a maximum time when the logic transition of a bit may be assigned to the transition window;

an earliest time when the logic transition of a bit is expected to occur;

a latest time when the logic transition of a bit is expected to occur; and

a nominal time when a logic transition of a bit is expected to occur.

5. The method of claim 4 wherein the operation of assigning each logic transition of the sequence of logic transitions to one of the plurality of transition time windows comprises:

assigning a first logic transition in the sequence of logic transitions to a first transition time window if the logic transition time falls between a first minimum time that a logic transition may be assigned to the first transition time window and a first maximum time that a logic transition may be assigned to the first transition time window.

6. The method of claim 5 wherein the plurality of transition time windows comprise a sequence of time windows arranged such the first transition time window with the first maximum time value is followed be a second transition time window with a minimum time value following the maximum time value of the first transition time window.

7. The method of claim 6 wherein the operation of assigning a first logic transition in the sequence of logic transitions to a first transition time window further comprises shifting the first logic transition to the second transition window if the logic transition time for the first logic transition exceeds the maximum time value for the first transition window.

8. The method of claim 7 wherein the operation of deriving the pattern of output bits from the integrated circuit as a function of the transition time of each logic transition in the sequence of logic transitions comprises generating a bit pattern that is a function of the shift of the first logic transition to the second transition window.

9. A method for testing a stream of digital information, comprising:

recording an arrival time of each logic transition in the stream; and

comparing the arrival time to an expected arrival time for each logic transition in the stream.

10. The method of claim 9 wherein one or more data unit intervals may occur between each logic transition in the stream, further comprising:

determining a logic value of the one or more data unit intervals occurring between each logic transition.

11. The method of claim 10 further comprising:

comparing the logic values of the all data unit intervals with expected logic values.

12. The method of claim 9 further comprising

determining a difference between the recorded arrival time of each logic transition with an expected arrival time of each logic transition.

13. The method of claim 12 further comprising:

comparing the difference between the recorded arrival time and the expected arrival time with limits.

14. The method of claim 12, further comprising:

distributing the differences between the recorded arrival times and the expected arrival times into histograms.

15. A method for receiving a logic data stream, comprising:

receiving a logic data stream comprising at least a first logic transition and a second logic transition;

recording a first time of the first logic transition;

recording a second time of the second logic transition;

generating a sequence of time intervals as a function of the specification of the logic data stream;

determining a time between the first time and the second time;

comparing the time between the first time and the second time with the sequence of time intervals; and

determining a bit pattern associated with the logic data stream as a function of the operation of comparing.

16. The method of claim 15, wherein the operation of generating a sequence of time intervals further comprises the operation of multiplying a unit interval time specified for the logic data stream by a sequence of integers.

17. The method of claim 15, wherein the operation of generating a sequence of time intervals further comprises recording times of a sequence of logic transitions in a second logic data stream.

18. The method of claim 17, wherein said second logic data stream is contemporaneous with the logic data stream.

19. The method of claim 15, wherein the operation of generating a sequence of time intervals is performed prior to the operation of receiving a logic data stream comprising at least a first logic transition and a second logic transition.

20. The method of claim 19, wherein the operation of generating a sequence of time intervals further comprises performing a logic simulation of an apparatus that generates said logic data stream.

21. The method of claim 20 wherein the apparatus comprises a device under test.

22. The method of claim 15 wherein the sequence of time intervals comprises a contiguous sequence of transition windows, each transition window comprising:

a minimum time value when a logic transition may be assigned to the transition window;

a maximum time value when the logic transition may be assigned to the transition window;

a nominal time value when the logic transition may be assigned to the transition window;

an earliest time value when the logic transition may be assigned to the transition window; and

a latest time value when the logic transition may be assigned to the transition window.

23. A method for testing a logic data stream, comprising:

recording a time of a first logic transition in the data stream;

recording a second time of a second logic transition in the data stream;

comparing a time interval between the time of the first logic transition and the time of second logic transition to a known sequence of possible interval times;

setting a data value determined by said first logic transition time corresponding to the specific interval time in said known sequence of possible interval times; and

comparing the data value to a predetermined expected data value.